REMARKS

Claim 19 is amended, no claims are canceled, and claims 22-24 are added; as a result, claims 1-24 are now pending in this application.

No new matter has been added through the amendments to claim 19, and no new matter has been added through new claims 22-24. Support for the amendments to claim 19 and for new claims 22-24 may be found throughout the specification, for example in the specification on page 15, line 14 through page 17, line 5, and in FIG. 6.

§*102 Rejection of the Claims*

Claims 19-21 were rejected under 35 U.S.C. § 102(e) as being unpatentable over Dobecki (U.S. 6,611,879).

Applicable Law

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W. L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131.

Claims 19-21 are not anticipated by Dobecki because Dobecki fails to shown the identical invention as contained in claims 19-21.

Claims 19-21 are not anticipated by Dobecki, because Dobecki fails to teach each of the elements included in claims 19-21 arranged as in claims 19-21. For example, claim 19 as now amended recites,

a send queue engine connected to the send queue context memory, the transmitter and the receiver, **wherein the send queue engine is connected to the send queue context memory by a first connection**; and

a receive queue engine partitioned from the send queue engine and connected to the receive queue context memory, the transmitter and the receiver, **wherein the receive queue engine is connected to the receive queue context memory by a second connection separate from the first connection**.

The Office Action on pages 5-6 lists various reference numbers from Dobecki that are cited as describing the elements included in claim 19. For example, the Office Action cites reference number 418 as disclosing a transmitter, reference number 424 as disclosing a receiver, reference number 312S as disclosing a send queue context memory, and reference number 428p as disclosing a send queue engine connected to the send queue context memory, the transmitter, and the receiver. Further, the Office Action cites reference number 312R as disclosing a receive queue context memory, and reference number 428d as disclosing a receive queue engine connected to the receive queue context memory and the transmitter and the receiver.

However, claim 19 as amended includes, "wherein the send queue engine is connected to the send queue context memory by a first connection" and further includes, "wherein the receive queue engine is connected to the receive queue context memory by a second connection **separate from** the first connection ." (Emphasis added). While Applicant does not admit that any of the reference numbers cited on pages 5-6 of the Office Action teach the elements as included in claim 19, the arrangement of the items associated with the reference numbers cited in the Office Action, for example as shown in FIG. 7 of Dobecki, are not arranged as recited in claim 19. Thus, these reference numbers, and the disclosure of Dobecki, fail to teach the elements of claim 19 as arranged in claim 19.

For example, reference number 312S (which the Office Action cites as disclosing a send queue context memory) is coupled to reference number 428P (which the Office Action cites as disclosing a send queue engine) through at least Edac/mem Contr 303, **CPU BUS 317**, DMA XMIT 418, and XMIT BUF 422, as shown in FIG. 7 of Dobecki. A similar arrangement occurs with respect to reference number 312R (which the Office Action cites as disclosing a receive queue context memory) which is coupled to reference number 428D (which the Office Action

cites as disclosing a received [sic] queue engine) through at least Edac/mem Contr 303, **CPU BUS 317**, DMA REC 424, and REC BUF 424, as shown in FIG. 7 of Dobecki.

Thus, Dobecki teaches that both block 312S and block 312R are coupled to the blocks 428P and 428D through CPU BUS 317. Therefore, Dobecki cannot teach "wherein the send queue engine is connected to the send queue context memory by a first connection" and "wherein the receive queue engine is connected to the receive queue context memory by a second connection **separate from** the first connection ," as recited in claim 19, even if the reference numbers cited in the Office Action represented the elements included in claim 19 (wherein again, Applicant does not admit that any of the reference numbers cited on pages 5-6 of the Office Action with respect to Dobecki represent the elements recited in claim 19).

Because Dobecki fails to teach each of the elements recited in claim 19 arranged as in claim 19, claim 19 is not anticipated by Dobecki.

Further, claims 20-21 depend from claim 19, and so include all of the elements recited in claim 19. Thus, Dobecki fails to teach each of the elements included in claims 20-21, as arranged in claims 20-21, and so claims 20-21 are not anticipated by Dobecki.

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of claims 19-21.

§103 Rejection of the Claims

Claims 1-7 and 10-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Muller et al. (U.S. 6,453,360) in view of Filepp et al. (U.S. 6,199,100). Applicant respectfully traverses the rejection of claims 1-7 and 10-16 because the Office Action fails to state a *prima facie* case of obviousness with respect to claims 1-7 and 10-16.

The proposed combination of Muller et al. and Filepp et al. fails to teach or suggest each of the elements included in claims 1-7 and 10-16.

Claims 1-7 and 10-16 are not obvious in view of the proposed combination of Muller et al. and Filepp et al. because the proposed combination of Muller et al. and Filepp et al. fails to teach or suggest each of the elements included in claims 1-7 and 10-16. For example, both claims 1 and 10 recite,

> for every **request packet transmitted by the network interface,**
> writing the packet sequence number **to a location in a circular send queue** pointed to by a write pointer and **setting a valid bit at said location**, wherein the valid bit is indicative of whether at least one response is expected. (Emphasis added).

In contrast, the Muller et al. reference concerns processing of packets after they are received by a Network Interface Circuit (NIC) in order to more efficiently transfer the received packet to a host computer or other communication device. (*See* Muller et al. at column 8, lines 55-58). This processing aspect of received packets is further emphasized in Muller et al. at column 10, lines 32-37 which states, "In the illustrated embodiment of the invention, a communication flow comprises one or more datagram packets from one source entity to one destination entity." (Emphasis added).

Thus, Muller et al. concerns the one way communication flow from one source entity to one destination entity, and the handling of the packets at the destination entity based on information included in the packet header for handling the packet once it arrives at the destination entity. Because Muller et al. describes the processing of received packets, Muller et al. fails to teach "for every **request packet transmitted by the network interface**, writing the packet sequence number **to a location in a circular send queue** pointed to by a write pointer and **setting a valid bit at said location**, wherein the valid bit is indicative of whether at least one response is expected," as recited in both claims 1 and 10.

Further, the Office Action on page 3 admits that Muller et al. fails to specifically disclose that the valid bit is indicative of whether at least one response is expected. In an attempt to supply the elements missing from Muller et al. and included in claims 1 and 10, the Office Action on page 3 relies on Filepp et al., wherein the Office Action on page 3 states,

> Filepp teaches the use of a "response expected" bit that is indicative of whether at least one response is expected to a packet. This bit is set when a response to the current packet is expected and cleared when no response is expected (at least Col 29, Lines 14-16; Col 36, Lines 18-27; Col 39, Lines 10-25).

However, Filepp et al. describes *headers* included in DIA implemented headers, that is, the messages sent between partners in a utility session.[1] Thus, the cited portions of Filepp et al.

[1] See e.g. Filepp et al. at column 24, lines 29-32.

relied on by the Office Action relate to the content of *message headers*. There is no disclosure in Filepp et al. of "for every request packet transmitted by the network interface, writing the packet sequence number to **a location in a circular send queue** pointed to by a write pointer and setting **a valid bit at said location**, wherein the valid bit is indicative of whether **at least one response is expected**," as recited in claims 1 and 10.

Instead, Filepp et al. at column 24, lines 53-55 states,

> In accordance with the invention **messages** conforming to DIA are composed of two functional parts: **message headers** and message text. (Emphasis added).

Further, Filepp et al. at column 25, lines 25-28 states,

> With regard to destination routing, the basic premise of DIA is that **each message flowing through network 10 carries a DIA header (FM0)** that identifies its source and destination ids. (Emphasis added).

And further, Filepp et al. at column 29, lines 1-16 states,

> In accordance with the invention, the DIA headers are arranged in a predetermined form base on their function. More particularly, **FMO headers, also known as Type "O" headers are required for every message** within the network. Header Type 0 provides information necessary for routing and message correlation. Its fields include:
> Header Length--Length of header data including length field.
> Header Type--Bit 0 is header concatenation flag.
> Bits 1-7 indicate current header type.
> Function Code--Contains message function.
> Data Mode--Indicates attributes of message data.
> The "response expected" bit should be turned off if no response is expected, for instance, when sending the response to a request. (Emphasis added).

Thus, Filepp et al. disclose information provided in FMO headers, the *FMO headers including* a "response expected" bit. However, a disclosure of information in headers included in *messages flowing through network 10* fails to teach or suggest each of the elements as recited in claims 1 and 10, including but not limited to,

> for every request packet transmitted by the network interface, writing the packet sequence number **to a location in a circular send queue** pointed to by a write pointer and **setting a valid bit at said location**, wherein the valid bit is indicative of whether at least one response is expected.

Because Filepp et al. fails to teach or suggest one or more of the elements included in claims 1 and 10 and missing from Muller et al., the proposed combination of Muller et al. and Filepp et al. fails to teach or suggest each of the elements included in claims 1 and 10. Thus, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 1 and 10.

Claims 2-7 depend from claim 1, and so include all of the elements recited in claim 1. Claims 11-16 depend from claim 10, and so include all of the elements recited in claim 10. Because the proposed combination of Muller et al. and Filepp et al. fails to teach or suggest all of the elements included in claim 1 and claim 10, the proposed combination of Muller et al. and Filepp et al. also fails to teach or suggest all of the elements included in claims 2-7 and 11-16. Thus, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 2-7 and 11-16.

The Office Action fails to state a prima facie case of obviousness by failing to show suggestion or incentive for forming the proposed combination of Muller et al. and Filepp et al.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The Office Action on page 4 states,

> This would have been an advantageous addition to the system taught by Muller since it would have allowed the packet processing devices to determine whether a response was expected to the packet being processed and act accordingly.

However, the very first sentence in the Abstract of Muller et al. states, "A high performance network interface is provided *for receiving a packet from a network* and transferring it to a host computer system. (Emphasis added). Thus as noted above, Muller et al. concerns processing of packets after they are *received* by a Network Interface Circuit (NIC) in order to more efficiently transfer the *received packet* to a host computer or other communication device. (*See* Muller et al. at column 8, lines 55-58).

The Office Action fails to point out any portion of Muller et al. where Muller et al. is concerned with determining "whether a response was expected to the packet being processed and act accordingly," as suggested on page 4 of the Office Action. Without this, the Office Action fails to show how the combined teaching of the references would have suggested the proposed combination of Muller et al. and Filepp et at.

By failing the meet the requirements as stated above for forming the proposed combination of Muller et al. and Filepp et al., the Office Action fails to state a *prima facie* case of obviousness with respect to claims 1-7 and 10-16.

For at least the reasons state above, Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of claims 1-7 and 10-16.

Allowable Subject Matter

Claims 8-9 and 17-18 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant acknowledges the allowable if rewritten indication as stated above for claims 8-9 and 17-18. However, based on at least the arguments presented above, Applicant believes claims 8-9 and 17-18 are allowable in their current form, and thus have not amended claims 8-9 and 17-18 at this time. Applicant respectfully requests allowance of claims 8-9 and 17-18.

Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at 612-371-2132 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 26th day of May, 2006.

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